WHAT IS CLAIMED IS:

1. A memory device comprising:

a memory cell including a plurality of active devices, which can be switched on by an applied threshold voltage;

a power line coupled to at least one storage node by at least one of the active devices; and

a virtual ground coupled to the at least one storage node by at least one other of the active devices;

wherein potentials of the power line and the virtual ground cause the plurality of active devices to be selectively operated in near subthreshold and/or superthreshold regimes in accordance with a mode of operation.

2. The device as recited in claim 1, wherein the mode of operation includes one of a standby mode and an access mode.

3. The device as recited in claim 2, wherein the

virtual ground is de-coupled from a global ground through a first device such that cell leakage from the cell raises the potential of the virtual ground during standby mode to reduce storage node leakage.

4. The device as recited in claim 2, wherein the virtual ground is connected to a global ground through a first device to increase a difference in potential during access mode operations.

5. The device as recited in claim 1, wherein the power line is boosted above a supply voltage by capacitive coupling to a wordline.

6. The device as recited in claim 5, wherein the mode of operation includes an access mode and a voltage difference between a boosted supply voltage and a ground is greater than or equal to about 3 times a threshold voltage of the active devices.

7. The device as recited in claim 1, wherein the mode of operation includes a standby mode and a voltage difference between a supply voltage and the virtual ground is less than or equal to about two times a threshold voltage of the active devices.

8. The device as recited in claim 1, wherein the device includes a static random access memory.

9. The device as recited in claim 1, wherein the plurality of actives devices includes six transistors.

10. The device as recited in claim 1, wherein near subthreshold operation includes subthreshold operation.

11. A static random access memory device comprising:

a memory cell including a plurality of transistors, which are active with an applied threshold voltage;

a power line coupled to storage nodes by first transistors; and

a virtual ground coupled to the storage nodes by second transistors;

wherein potentials of the power line and the virtual ground selectively cause the plurality of transistors to be operated in near subthreshold and/or superthreshold regimes in accordance with a mode of operation.

12. The device as recited in claim 11, wherein the mode of operation includes one of a standby mode and an access mode.

13. The device as recited in claim 12, wherein the virtual ground is de-coupled from a global ground through a third device such that cell leakage from the cell raises the potential of the virtual ground during standby mode to reduce storage node leakage.

14. The device as recited in claim 12, wherein the virtual ground is connected to a global ground through a fourth device to increase a difference in potential during

access mode operations.

15. The device as recited in claim 11, wherein the power line is boosted above a supply voltage by capacitive coupling to a wordline.

16. The device as recited in claim 15, wherein the mode of operation includes an access mode and a voltage difference between a boosted supply voltage and a ground is greater than or equal to about 3 times a threshold voltage of the plurality of transistors.

17. The device as recited in claim 11, wherein the mode of operation includes a standby mode and a voltage difference between a supply voltage and the virtual ground is less than or equal to about two times a threshold voltage of the plurality of transistors.

18. The device as recited in claim 11, wherein the plurality of transistors includes six transistors.

19. The device as recited in claim 11, wherein near subthreshold operation includes subthreshold operation.

20. A method for operating a transregional static random access memory (SRAM) device, comprising the steps of:

providing a virtual ground in an SRAM cell, which is selectively decoupled from a global ground by a first device;

providing a powerline which is capacitively coupled to a wordline such that power is boosted above a supply voltage when the wordline is activated; and

maintaining a voltage difference between the power line and one of the virtual ground and the ground to selectively operate devices of the SRAM in a near subthreshold or superthreshold regime in accordance with a mode of operation.

21. The method as recited in claim 20, wherein the

step of maintaining includes the step of maintaining a voltage difference between the power line and the virtual of less than or equal to about 2 times the threshold voltage of the devices during a standby mode.

22. The method as recited in claim 20, wherein the step of maintaining includes the step of maintaining a voltage difference between the power line and the global ground of greater than or equal to about 3 times the threshold voltage of the devices in an access mode.

23. The method as recited in claim 20, wherein the step of providing a virtual ground in an SRAM cell which is selectively decoupled from a global ground by a first device includes coupling the global ground to the virtual ground during an access mode.

24. The method as recited in claim 20, wherein the step of providing a virtual ground in an SRAM cell, which is selectively decoupled from a global ground by a first

device, includes restoring the virtual ground to a nonzero potential during a standby mode.

25. The method as recited in claim 20, wherein the near subthreshold operation of the devices is associated with a standby mode and a superthreshold operation of the devices is associated with an access mode.